The Cisco 7200 Series Routers

The 7200 router was the first Cisco router designed to use the now common, industry-standard PCI bus. The 7200 series has a modular architecture that uses replaceable media interfaces called *port adapters* and an interchangeable main processor called the *Network Processing Engine*(NPE).

The 7200 is available in several configurations based upon combinations of chassis models and available NPEs. The number of slots and the type of midplane installed distinguish the chassis models. At the time of this writing, two midplane designs are available for the 7200 series chassis:

- **Original midplane—**

  Contains two PCI buses running at 25 MHz. Each bus connects to half the slots in a chassis. This midplane supports all NPEs except the NPE-300.

- **VXR midplane—**

  Contains two dual-speed PCI buses capable of running at either 25 or 50 MHz. Each bus connects to half the slots in a chassis. In addition, the midplane contains a TDM (time division multiplexing) switch with two dedicated links, called *Multiservice Interchange Connections*, to each chassis slot. This midplane primarily is intended for use with the NPE-300, but it supports all NPEs.

The 7200 series chassis is available in two-slot, four-slot, and six-slot versions. The following list examines the 7200 series chassis configurations:

- **7202—**

  A two-slot chassis used in some niche applications. This router has the original 25-MHz midplane and supports only the NPE-150.

- **7204—**

  A four-slot chassis with the original midplane.

- **7206—**

  A six-slot chassis with the original midplane.

- **7204VXR—**

  A four-slot chassis with the VXR midplane.

- **7206VXR—**

  A six-slot chassis with the VXR midplane.

Several NPEs have been developed for the 7200 series router; all feature a MIPS-compatible CPU. Most are interchangeable, with a few exceptions. For example, the two-slot 7202 chassis supports only the NPE-150, and the NPE-300 is supported only in a chassis with the VXR midplane. Each NPE is distinguished by its CPU speed and the type of memory it contains:

- **NPE-100—**

An early 7200 series NPE with a VR4700-100 100-MHz CPU and DRAM memory only (no SRAM).

- **NPE-150—**

  Contains a VR4700-150 CPU running at 150 MHz. Uses DRAM for main memory and both DRAM and SRAM for packet buffers.

- **NPE-175—**

  Contains an RM5270-200 CPU running at 200 MHz with a 2 Mb unified cache. Uses SDRAM for main memory and packet buffers.

- **NPE-200—**

  Contains a VR5000-200 CPU running at 200 MHz. Uses DRAM for main memory and both DRAM and SRAM for packet buffers.

- **NPE-225—**

  Contains an RM5271-262 CPU running at 262 MHz with a 2 Mb unified cache. Uses SDRAM for main memory and packet buffers.

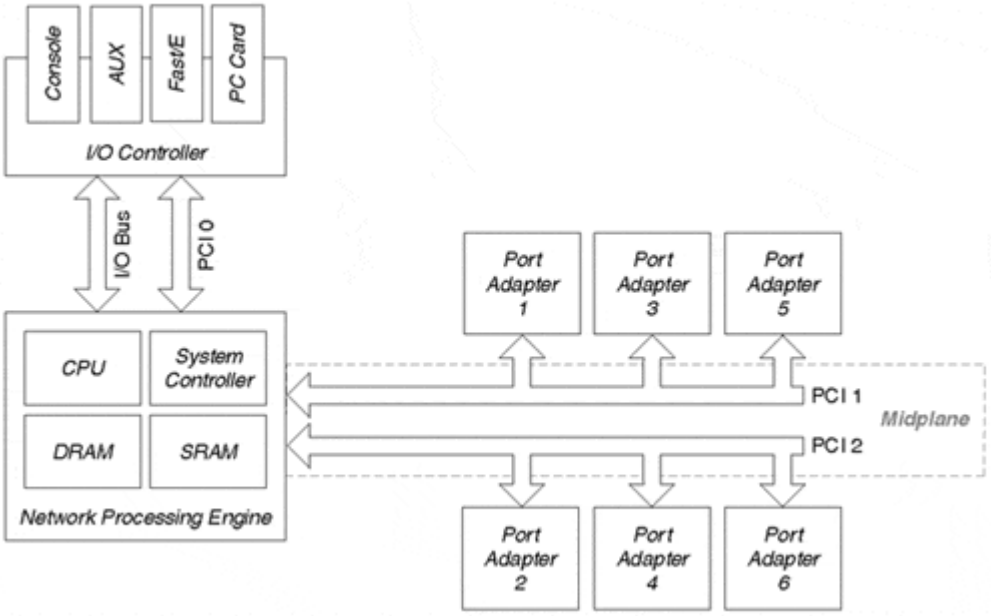
- **NPE-300—**

  Contains an RM7000-300 CPU running at 300 MHz and two independent banks of SDRAM memory. This NPE has two separate PCI/memory bus controllers allowing concurrent access to SDRAM from two different port adapters, providing improved performance. The NPE-300 also operates the PCI busses at 50 MHz and requires the VXR midplane.

Hardware Architecture

The 7200 series hardware architecture varies from model to model and depends upon the combination of chassis and NPE, but it generally can be separated into two major designs: routers with the original midplane and an early NPE (NPE-100, NPE-150, NPE-200), and routers with the VXR midplane and an NPE-300. Figure 5-3 illustrates the components of a Cisco 7200 series router employing the original midplane design. This particular example illustrates a 7206 with an NPE-150.

Figure 5-3. Cisco 7200 Architecture—Original Midplane



The following list explains the Cisco 7200 components as illustrated in Figure 5-3.

- **NPE—**

  Contains the main memory, the CPU, the PCI memory (SRAM, except on the NPE-100 which uses DRAM), and the control circuitry for the PCI busses. As noted previously, several types of NPEs are available—all are supported with the original midplane except the NPE-300.

- **PCI Bus—**

  There are three PCI data busses in a Cisco 7200: PCI 0, PCI 1, and PCI 2. PCI 1 and PCI 2 extend from the NPE to the midplane and interconnect the media interfaces (port adapters) to the CPU and the memory on the NPE. PCI 0 is separate and is used to connect the media interface and the PCMCIA on the I/O controller to the CPU and the memory on the NPE. Running at 25 MHz, PCI 0, PCI 1, and PCI 2 provide up to 800 Mbps in bandwidth each.

- **I/O bus—**

  Interconnects the non-PCI components on the I/O Controller (console port, AUX port, NVRAM, Boot ROM, and Boot FLASH) to the CPU on the NPE.

- **Port Adapters (PAs)—**

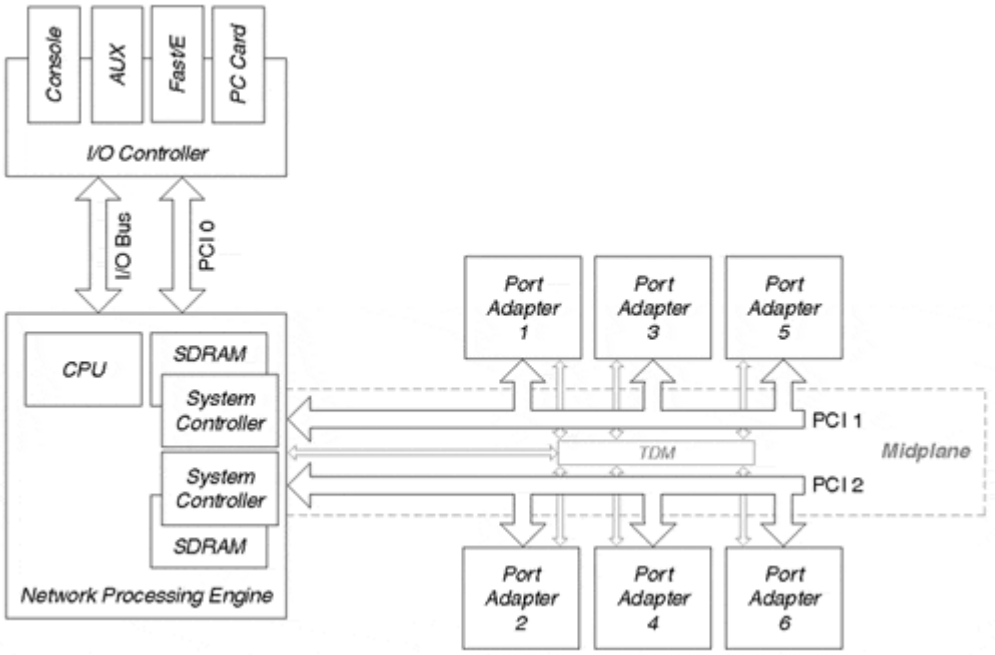
  These are modular interface controllers that contain circuitry to transmit and receive packets on the physical media. These are the same port adapters used on the VIP processors on a Cisco 7500 series router. Both platforms support most port adapters, but there are some exceptions.

- **I/O Controller—**

  Provides the console connection, the auxiliary connection, the NVRAM, the Boot ROM, the Boot FLASH, and a built-in interface controller—either an Ethernet or Fast Ethernet interface. The I/O Controller also provides access to the Flash memory cards in the PCMCIA card slot via PCI bus 0.

Figure 5-4 illustrates the components of the Cisco 7200VXR hardware architecture. This particular example illustrates a 7206VXR with an NPE-300.

Figure 5-4. Cisco 7200VXR Architectural Components



The following list explains the Cisco 7200VXR components as illustrated in Figure 5-4:

- **Network Processing Engine—**

  Contains the main memory, the CPU, the PCI memory, and the PCI bus control circuitry. The NPE-300 has two PCI bus controllers and two independent banks of SDRAM used for both main memory and packet memory.

- **PCI Bus—**

  Three PCI data busses exist in a Cisco 7200VXR: PCI 0, PCI 1, and PCI 2. PCI 1 and PCI 2 extend to the midplane and interconnect the media interfaces (port adapters) to the CPU and the memory on the NPE. PCI 0 is separate and is used to connect the media interface and the PCMCIA on the I/O Controller to the CPU and the memory on the NPE. PCI 0 runs at 25 MHz. PCI 1 and PCI 2 run at 50 MHz when a 50 MHz–capable NPE is installed (like the NPE-300 in this example); otherwise, they run at 25 MHz.

- **TDM switch—**

  The midplane contains a *time division multiplexing* (TDM) switch with two dedicated connections to each chassis slot. The TDM switch supports interconnection between port adapters that have TDM interfaces.

- **I/O bus—**

  Interconnects the non-PCI components on the I/O Controller (console port, AUX port, NVRAM, Boot ROM, and Boot FLASH) to the CPU on the NPE.

- **Port Adapters (PAs)—**

  These are the same port adapters used on the non-VXR 7200 routers. However, some PAs that require the TDM switch are supported only on the 7200VXR. The 7200VXR supports both legacy PAs with a 25-MHz internal PCI speed and 50 MHz PAs; any bus speed mismatch is resolved by the bus isolation between the midplane and the PAs.

- **I/O Controller—**

Provides the console connection, the auxiliary connection, the NVRAM, the Boot ROM, the Boot FLASH, and a built-in interface controller—either an Ethernet or Fast Ethernet interface. The I/O Controller also provides access to the Flash memory cards in the PCMCIA card slot via PCI bus 0.

Memory

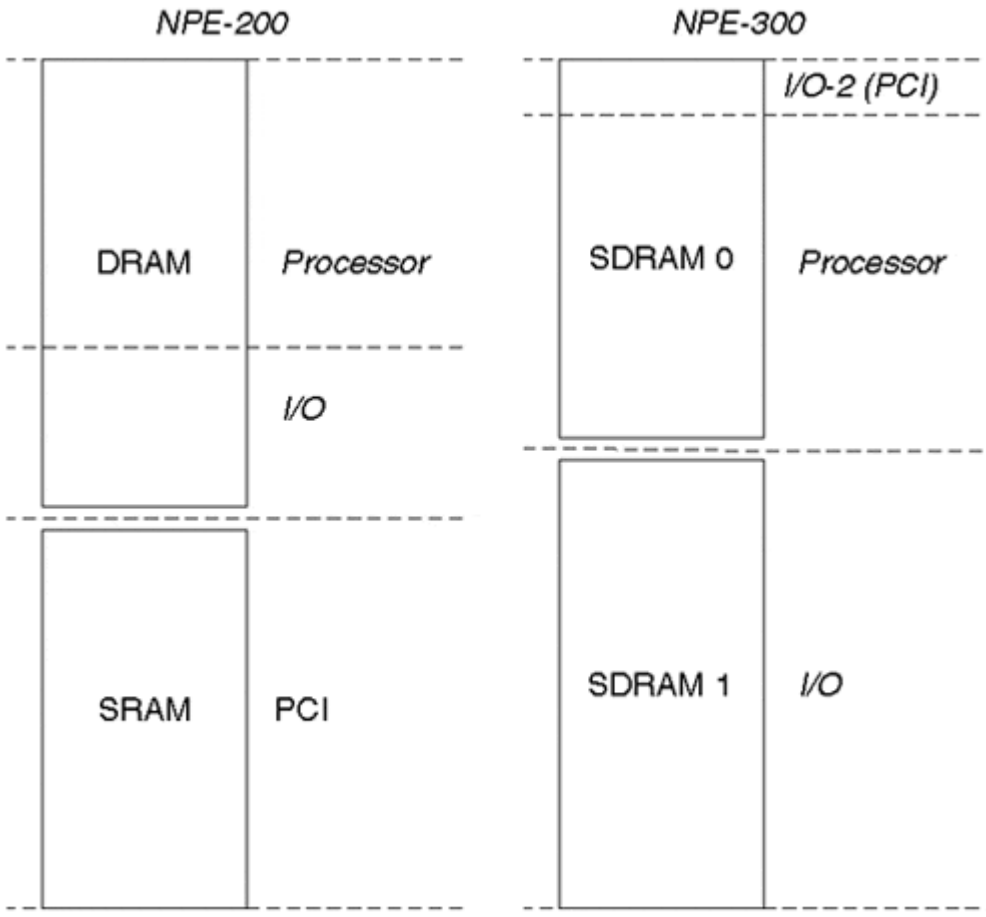
The 7200 series routers use DRAM, SDRAM, and SRAM memory on the NPE in various combinations depending on the NPE model. Three memory pools divide the available memory: the standard *processor* pool, the *I/O*pool, and the *PCI*pool (*I/O-2*on NPE300). Example 5-2 illustrates some **show memory** command output showing these three pools. The first is from an NPE-200 and the other is from an NPE-300.

Example 5-2. show memory Command Output Displays Memory Pool Information for 7200 Series Routers

router-NPE-200#**show memory** Head Total(b) Used(b) Free(b) Lowest(b) Largest(b) Processor 61BEBC60 96551840 7287388 89264452 88777932 88547216 I/O 7800000 8388608 901616 7486992 7463324 7480508 PCI 4B000000 4194304 993276 3201028 2227180 2702716 router-NPE-300#**show memory** Head Total(b) Used(b) Free(b) Lowest(b) Largest(b) Processor 612A02A0 106298720 7408336 98890384 98748252 98836460 I/O 20000000 33554432 3604696 29949736 29925740 29949692 I/O-2 7800000 8388608 35608 8353000 8353000 8352956

Figure 5-5 illustrates the memory pools shown in Example 5-2. Figure 5-5 also shows how the available memory is allocated to the pools on these two sample NPEs.

Figure 5-5. Memory Types



The following sections examine how IOS distributes available memory between the pools.

Processor Memory

The processor memory pool is used for storing the IOS code, general data structures (such as the routing table), and the system buffers. The entire memory pool is allocated from the DRAM region on the NPE-100, the NPE-150, and the NPE-200; the SDRAM region on the NPE-175 and the NPE-225; and SDRAM bank 0 on the NPE-300.

I/O Memory

The I/O memory pool is used for particle pools. The interface private particle pools are allocated from this memory as well as the public particle pool *normal*.

On NPE-100, NPE-150, and NPE-200 platforms, this memory pool is created in DRAM, so it's used primarily to allocate private particle pools for slower speed interfaces. The size of I/O memory is dependent on the total amount of DRAM memory available on the NPE. For example, on an NPE-150, the following set of conditions determine the I/O memory:

- An NPE-150 with 16 MB total DRAM gets 4 MB allocated to I/O memory.
- An NPE-150 with between 24 MB and 48 MB of DRAM gets 6 MB allocated to I/O memory.
- An NPE-150 with more than 48 MB of DRAM gets 8 MB allocated to I/O memory.

Other NPEs use different formulas for determining how much DRAM should be used for I/O memory, too many to list here.

On the NPE-300, the I/O memory pool is created in SDRAM bank 1 and is fixed at 32 MB. All private interface particle pools are created in I/O memory on this NPE, regardless of the media speed.

PCI Memory

The PCI memory pool is used for interface receive and transmit rings. It also is used to allocate private interface particle pools for high-speed interfaces in some cases. On NPE-175, NPE-225, and NPE-300 systems, this pool is created in SDRAM. On NPE-150 and NPE-200 systems, it is created entirely in SRAM.

PCI memory is generally a small pool. As you can see from Example 5-2, the NPE-200 has only 4 MB of PCI memory and the NPE-300 has approximately 8 MB, labeled I/O-2.

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